WHAT IS CLAIMED IS:

1. A system for waiving a verification check associated with a circuit design, comprising:

a first engine for integrating waiver options associated with said circuit design's design objects into a hierarchical verification tree having said verification check, said waiver options populating at least one waiver database;

responsive to a verification check violation, a second engine for traversing a portion of said hierarchical verification tree to determine a list of applicable waivers; and

a third engine for resolving said list of applicable waivers to determine the disposition of said verification check violation.

2. The system as recited in claim 1, wherein said at least one waiver database comprises a global waiver database that specifies waiver options applicable to at least a portion of said circuit design.

3. The system as recited in claim 1, wherein said at least one waiver database comprises a local waiver database that specifies waiver options applicable to at least a portion of said circuit design.

4. The system as recited in claim 1, wherein said waiver options include a waiver to waive said verification check violation.

5. The system as recited in claim 1, wherein said waiver options include an enabler to enable reporting of said verification check violation.

6. The system as recited in claim 1, wherein said design objects comprise an object selected from the group consisting of latch query design objects, dynamic logic query design objects, and informational query design objects.

7. The system as recited in claim 1, wherein said verification check violation relates to a verification query selected from the group consisting of Design Rules Checking (DRC) queries, Electrical Rules Checking (ERC) queries, functional verification queries, timing verification queries, and behavioral verification queries.

8. The system as recited in claim 1, wherein said third engine is operable to present said resolved list of applicable waivers to a design engineer via an interface.

9. A method for waiving a verification check associated with a circuit design, comprising:

grouping verification checks into a hierarchical verification tree;

creating at least one waiver database specifying waiver options for different verification checks on a design object by design object basis;

integrating said waiver options into said hierarchical verification tree;

responsive to a verification check violation, traversing a portion of said verification tree to determine a list of applicable waivers; and

resolving said list of applicable waivers to determine the disposition of said verification check violation.

10. The method as recited in claim 9, wherein the operation of creating at least one waiver database further comprises creating a global waiver database that specifies waiver options applicable to at least a portion of said circuit design.

11. The method as recited in claim 9, wherein the operation of creating at least one waiver database further comprises creating a local waiver database that specifies waiver options applicable to at least a portion of said circuit design.

12. The method as recited in claim 9, wherein the operation of resolving said list of applicable waivers further comprises waiving said verification check violation.

13. The method as recited in claim 9, wherein the operation of resolving said list of applicable waivers further comprises reporting said verification check violation.

14. The method as recited in claim 9, wherein the operation of grouping verification checks into a hierarchical verification tree is based on a query classification hierarchy.

15. The method as recited in claim 9, wherein said verification check violation relates to a verification query selected from the group consisting of Design Rules Checking (DRC) queries, Electrical Rules Checking (ERC) queries, functional verification queries, timing verification queries, and behavioral verification queries.

16. The method as recited in claim 9, further comprising presenting said resolved list of applicable waivers to a design engineer via an interface.

17. A computer-readable medium operable with a computer platform for supporting a hierarchical query verification tool associated with a circuit design, the medium having stored thereon:

instructions for grouping verification checks into a hierarchical verification tree;

instructions for creating at least one waiver database specifying waiver options for different verification checks on a design object by design object basis;

instructions for integrating said waiver options into said hierarchical verification tree;

instructions, responsive to a verification check violation, for traversing a portion of said verification tree to determine a list of applicable waivers; and

instructions for resolving said list of applicable waivers to determine the disposition of said verification check violation.

18. The computer-readable medium as recited in claim 17, wherein the instructions for creating at least one waiver database further comprise instructions for creating a global waiver database that specifies waiver options applicable to at least a portion of said circuit design.

19. The computer-readable medium as recited in claim 17, wherein the instructions for creating at least one waiver database further comprise instructions for creating a local waiver database that specifies waiver options applicable to at least a portion of said circuit design.

20. The computer-readable medium as recited in claim 17, wherein the instructions for resolving said list of applicable waivers further comprise instructions for waiving said verification check violation.

21. The computer-readable medium as recited in claim 17, wherein the instructions for resolving said list of applicable waivers further comprise instructions for enabling said verification check violation.

22. The computer-readable medium as recited in claim 17, wherein said hierarchical verification tree is based on a query classification hierarchy.

23. The computer-readable medium as recited in claim 17, wherein said verification check violation relates to a verification query selected from the group consisting of Design Rules Checking (DRC) queries, Electrical Rules Checking (ERC) queries, functional verification queries, timing verification queries, and behavioral verification queries.

24. The computer-readable medium as recited in claim 17, further comprising instructions for presenting said resolved list of applicable waivers to a design engineer via an interface.

25. A verification check waiver system, comprising:

means for grouping verification checks into a hierarchical verification tree;

means for creating at least one waiver database specifying waiver options for different verification checks on a design object by design object basis;

means for integrating said waiver options into said hierarchical verification tree;

means, responsive to a verification check violation, for traversing a portion of said verification tree to determine a list of applicable waivers; and

means for resolving said list of applicable waivers to determine the disposition of said verification check violation.

26. The verification check waiver system as recited in claim 25, wherein said means for creating at least one waiver database further comprises means for creating a global waiver database that specifies waiver options applicable to at least a portion of said circuit design.

27. The verification check waiver system as recited in claim 25, wherein said means for creating at least one waiver database further comprises means for creating a local waiver database that specifies waiver options applicable to at least a portion of said circuit design.

28. The verification check waiver system as recited in claim 25, wherein said means for resolving said list of applicable waivers further comprises means for waiving said verification check violation.

29. The verification check waiver system as recited in claim 25, wherein said means for resolving said list of applicable waivers further comprises means for enabling said verification check violation.

30. The verification check waiver system as recited in claim 25, wherein said hierarchical verification tree is based on a query classification hierarchy.

31. The verification check waiver system as recited in claim 25, wherein said verification check violation relates to a verification query selected from the group consisting of Design Rules Checking (DRC) queries, Electrical Rules Checking (ERC) queries, functional verification queries, timing verification queries, and behavioral verification queries.

32. The verification check waiver system as recited in claim 25, further comprising means for presenting said resolved list of applicable waivers to a design engineer via an interface.